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EXAMINER	
PARKER, KENNETH	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/747,744	WU ET AL.	
	Examiner	Art Unit	
	Kenneth A. Parker	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12/23/03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 1-12 are objected to because of the following informalities: The term "expanding" used should have been "extending". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 6-8 are rejected under 35 U.S.C. 102(b) as being by Yamazaki et al 5933205.

Claim 1 is a method stabilizing parasitic capacitance in an LCD device, however is written to a method of making an LCD pixel. As there is no way to tell if a given structure is more or less stable then another structure, the language "stabilizing parasitic capacitance" is not given any significant weight as it is a comparison to an unspecificed device. Most of the listed steps are mere statements of providing the layers except the photolithography step. As photolithography using a photomask was

substantially the only method ever used to make LCD active matrixes, the limitation is either inherent or obvious as it was the only way employed and therefore one of ordinary skill would expect that the method had the benefit of established proceedures, supply chain and was known to work for its intended purpose. As the other elements are the steps of proving the parts, the parts of claim 1 are shown in the reference as follows:

providing a substrate (50);

forming a plurality of transversely expanding (extending) gate lines (3, 66) on the substrate;

forming a first insulating layer 65 on the substrate and the gate lines (first is understood to be a label, not implying there are no other insulators below it) ;

performing a photolithography procedure using a photomask (steps associated with 7f and 7g, described in column 8) to form a plurality of longitudinally expanding (extending) data lines 4, 74 and a plurality of metallic light shield layers 76 (any metal is a shield, and there is one per pixel) on part of the first insulating layer,

wherein the metallic light shield layers are located on both sides of the data line (pixels repeat or there is no display- so being on both sides is required and therefore inherent);

forming a second insulating layer 77 on the metallic light shield layers and the data lines;

and forming transparent conductive layers 24 (multiple pixels is required for display, so themultiple layers is inherent) on part of the second insulating layer.

The reference shows regarding 2 conductive plugs (the stem portion shown in figure 7I) penetrating the second insulating layer to electrically connect the metallic light shield layers and the transparent conductive layers.

The reference shows regarding claim 3 wherein the substrate is a glass substrate (glass is in column 4, lines 35-45).

The reference shows regarding 4 the first insulating layer is a silicon oxide (SiO.sub.x) layer (column 7, lines 35-45).

The reference shows regarding 6 the metallic light shield layers and the data lines comprise Al and/or Mo (column 8, lines 4-15) .

The reference shows regarding 7 the transparent conductive layers are ITO (indium tin oxide) or IZO (indium zinc oxide) layers (column 8, lines 15-22).

The reference shows regarding 8 the metallic light shield layers and the transparent conductive layers are equipotential (the transparent pixels are conductors, so in the same sense as applicant's they are equipotental).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 5, 9- 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al 5933205 in view of Rho 6243146.

Claim 9, 5 and the dependent claims are a method stabilizing parasitic capacitance in an LCD device, however is written to a method of making an LCD pixel. As there is no way to tell if a given structure is more or less stable then another structure, the language "stabilizing parasitic capacitance" is not given any significant weight as it is a comparison to an unspecificed device. Most of the listed steps are mere statements of providing the layers except the photolithography step. As photolithography using a photomask was substantially the only method ever used to make LCD active matrixes, the limitation is either inherent or obvious as it was the only way employed and therefore one of ordinary skill would expect that the method had the benefit of established proceedures, supply chain and was known to work for its intended purpose. As the other elements are the steps of proving the parts, the parts of claim 9, 5 and the dependent claims are shown in the reference as follows:

providing a glass substrate (50)(glass is in column 4, lines 35-45).

forming a plurality of transversely expanding (extending) gate lines (3, 66) on the substrate;

forming a first insulating layer 65 (SiO- column 7, lines 35-45). on the substrate and the gate lines (first is understood to be a label, not implying there are no other insulators below it) ;

performing a photolithography procedure using a photomask (steps associated with 7f and 7g, described in column 8) to form a plurality of longitudinally expanding (extending) data lines 4, 74 and a plurality of metallic light shield layers 76 (any metal is a shield, and there is one per pixel) on part of the first insulating layer,

wherein the metallic light shield layers are located on both sides of the data line (pixels repeat or there is no display- so being on both sides is required and therefore inherent); forming a second insulating layer 77 (SiO not shown but discussed below) on the metallic light shield layers and the data lines;
and forming transparent conductive layers 24 (multiple pixels is required for display, so themultiple layers is inherent) on part of the second insulating layer.

Regarding claims 5, 9 and those dependent from 9, lacking from the disclosure is that the second insulator is SiOx. The second insulator of Yamaki is an organic flattening layer. SOG (spun on glass are spun on layers including SiO, and were functionally equivalent alternatives. Rho et al discloses polyimide (an organic layer), as an alternative to SOG (a spun on SiO layer- column 5, lines 1-6). The teaching of Rho et al is applicable because it deals with a flattening layer below the pixel for an LCD. Therefore, one of ordinary skill would have found motivation, reason, or suggestion to modify the primary reference as one of ordinary skill would have recognized that SOG layers were suitable for the intended purpose as they were recognized as functionally equivalent alternative (which were further known to be low cost).

The reference shows regarding 10 the metallic light shield layers and the data lines are equipotential (see above discussion of claim 8).

The reference shows regarding 11 wherein the metallic light shield layers and the data lines comprise Al and/or Mo (see above discussion of claim 7).

The reference shows regarding 12 the transparent conductive layers are ITO (indium tin oxide) or IZO (indium zinc oxide) layers (see above discussion of claim 6).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth A. Parker whose telephone number is 571-272-2298. The examiner can normally be reached on M-F 10:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on 571-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kenneth A Parker
Primary Examiner
Art Unit 2871